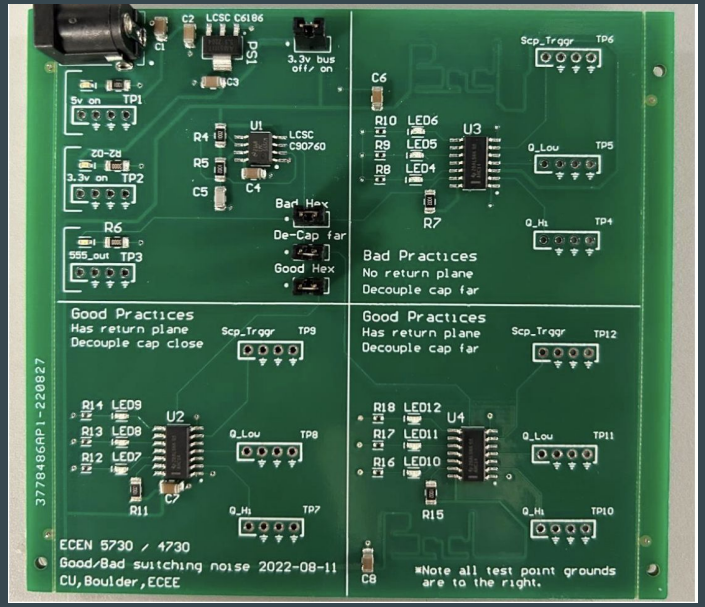
Connor Sorrell—Lab 15 Ecen 3730

Good



Bad

Good/Far

Investigating good vs. bad design on a switching noise board.
Specifically, comparing 3 identical circuits but with different layouts.

	Rise Time	Fall Time	Voltage Collapse Q_Hi	Ground Bounce Q_Lo
Return Plane w/ Close Decoupling Cap. **GOOD**	~1.5 ns	~1.3ns	**0.95 V** Rising Edge, **0.43 V** Falling Edge	**0.45 V** Rising Edge, **0.45 V** Falling Edge
Return Plane w/ Far Decoupling Cap. **GOOD/FAR**	~3.2 ns **(2x slower)***	~1.4 ns **(~same)**	**1.5 V** Rising Edge **(1.6x worse)** , **2.4 V** Falling Edge **(5.6x worse)**	**0.28 V** Rising Edge, **(40% better)** , **0.74 V** Falling Edge **(1.6x worse)**
No Return Plane w/ Far Decoupling Cap **BAD**	~3 ns **(2x slower)**	~3.5 ns **(2.7x slower)**	**1.4 V** Rising Edge **(1.5x worse)** , **2.8 V** Falling Edge **(6.5x worse)**	**0.86 V** Rising Edge **(2x worse)** , **3.4 V** Falling Edge **(7.5x worse)**

*Slower, worse, etc. are in reference to the GOOD design

Summary

Rise/Fall Times:

- The GOOD design had ~**2x faster rise times** and **~3x faster fall times** compared to the BAD design.

Voltage Collapse:

- The GOOD design had **50%–85% less voltage collapse** than the BAD design.
- The GOOD/FAR design was significantly worse than GOOD, especially for **voltage collapse (5.6x worse)** .

Takeaways:

- **Good design practices significantly improve signal integrity** —optimized layout reduced **rise/fall times by up to 2.7x** and **minimized voltage collapse on quiet nodes by up to 7.5x** , demonstrating the critical impact of proper return paths and proper placement of decoupling capacitors
- **Poor layout dramatically increases noise and delays** —excessive loop inductance and shared return paths caused **longer rise times, severe QHi/QLo voltage collapse (up to 6.5x worse), and greater overall signal degradation**

Supporting Data & Measurements

Rising Edge

Yellow Waveform: GOOD Design (~1.5 ns)
Green Waveform: Good/Far Design (~3.2 ns)
Ref Waveform: BAD Design (~3 ns)

Falling Edge

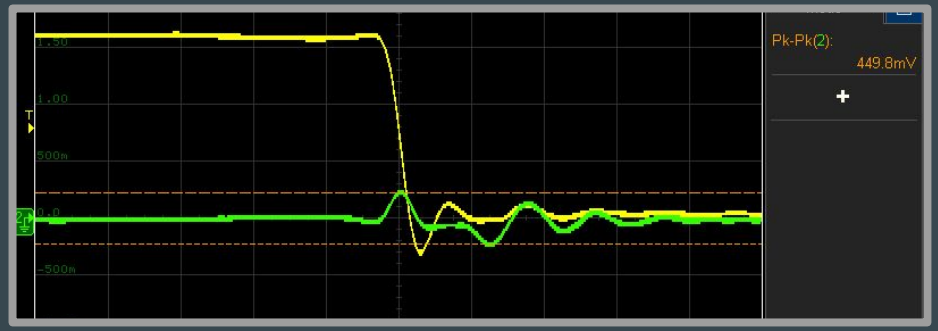
GOOD Design (~1.3 ns)
Good/Far Design (~1.4 ns)
BAD Design (~3.5 ns)

GOOD Design

Yellow Waveform: 555 Output trig'd on Edge

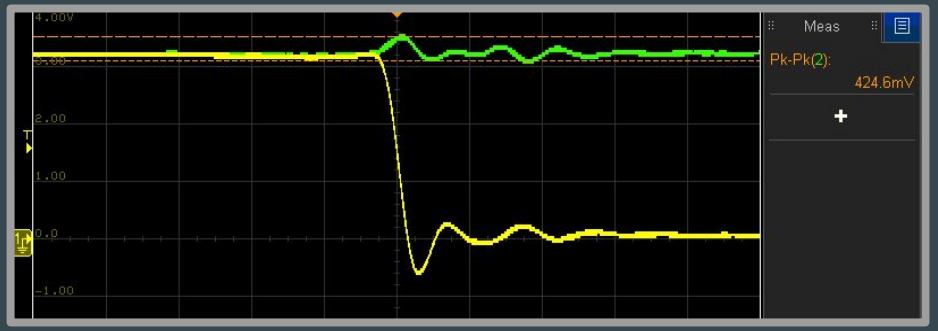
Green Waveform: Noise on Rail

Ground Bounce Quiet Low:

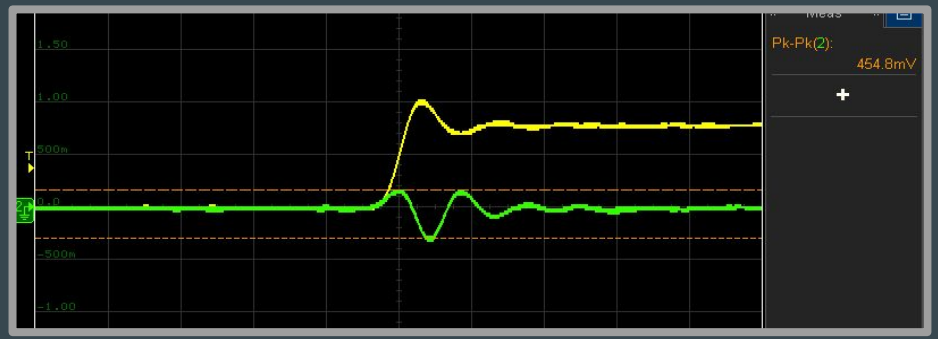


Falling Edge noise: ~450 mV

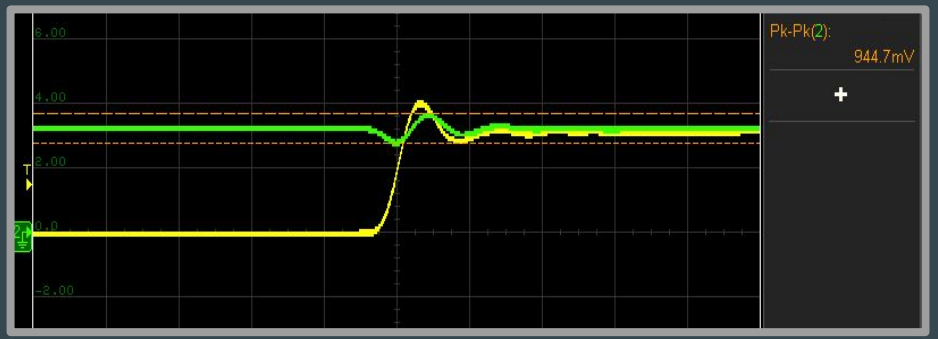
Voltage Collapse Quiet High:



Falling Edge noise: ~425 mV



Rising Edge noise: ~455 mV



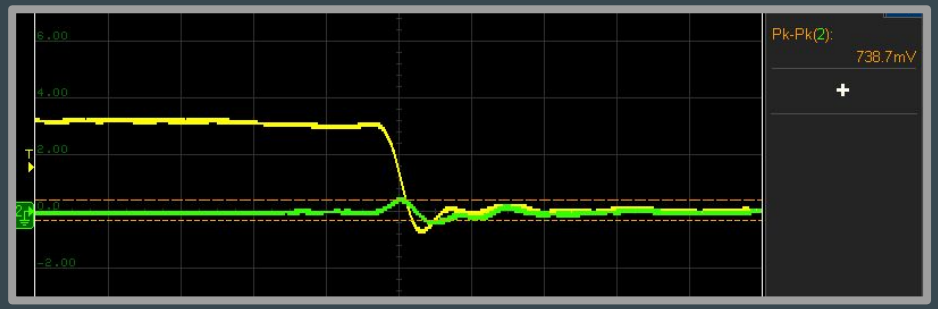
Rising Edge noise: ~950 mV

Good/Far Design

Yellow Waveform: 555 Output trig'd on Edge

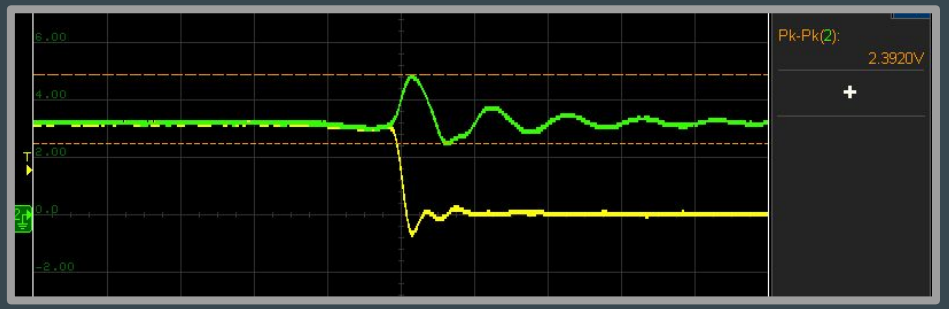
Green Waveform: Noise on Rail

Ground Bounce Quiet Low:

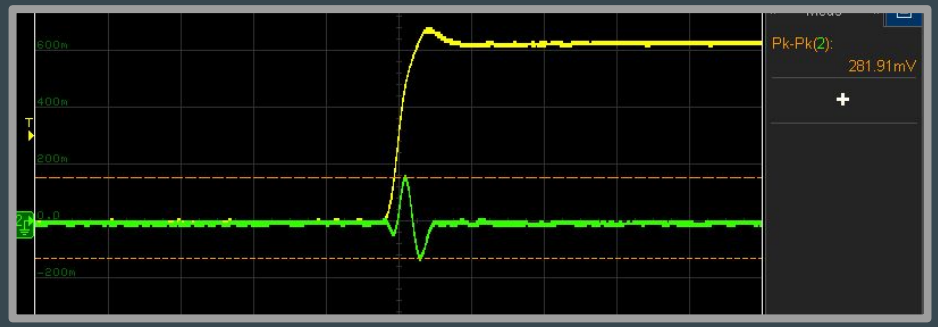


Falling Edge noise: ~740 mV

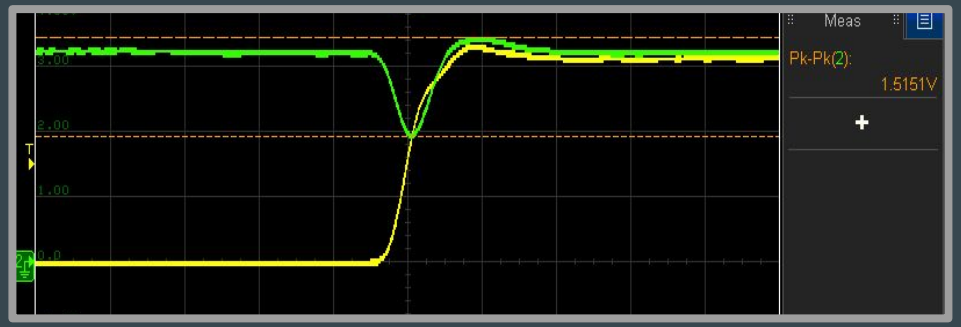
Voltage Collapse Quiet High:



Falling Edge noise: ~2.4 V



Rising Edge noise: ~282 mV



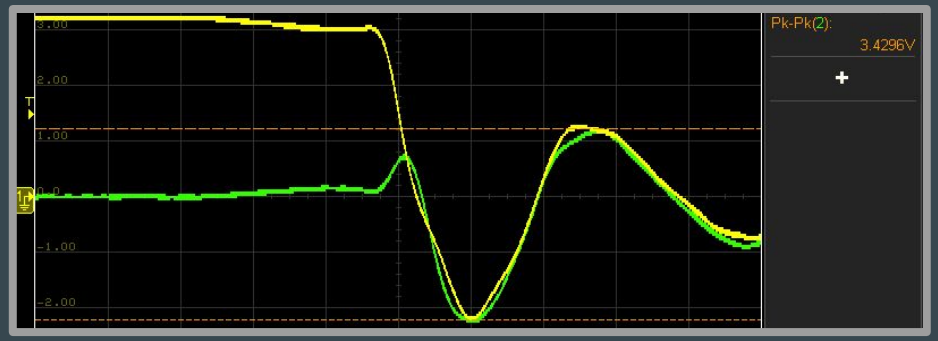
Rising Edge noise: ~1.5 V

BAD Design

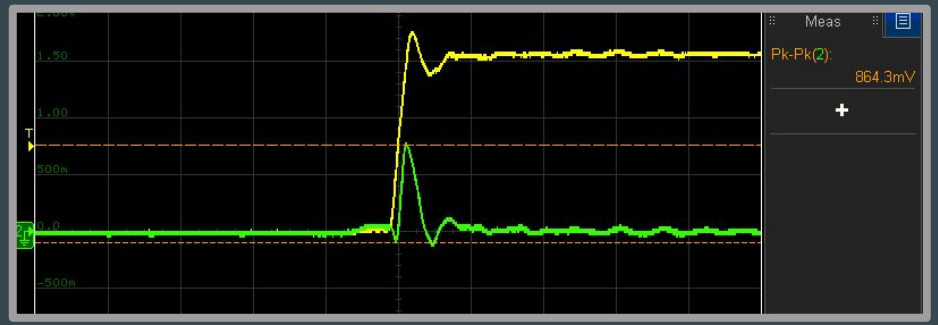
Yellow Waveform: 555 Output trig'd on Edge

Green Waveform: Noise on Rail

Ground Bounce Quiet Low

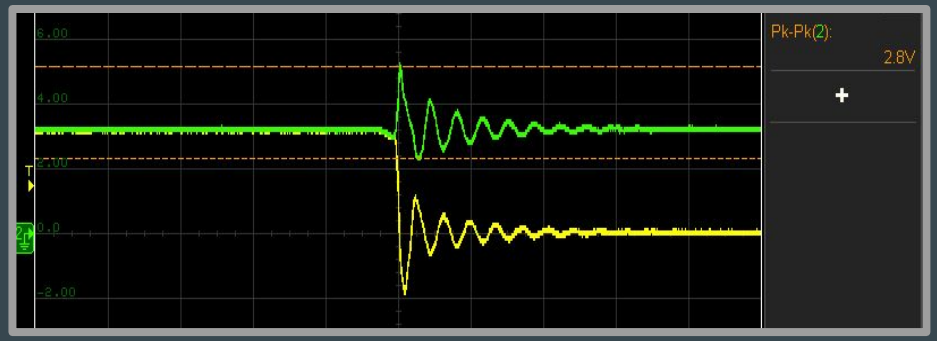


Falling Edge noise: ~3.4 V

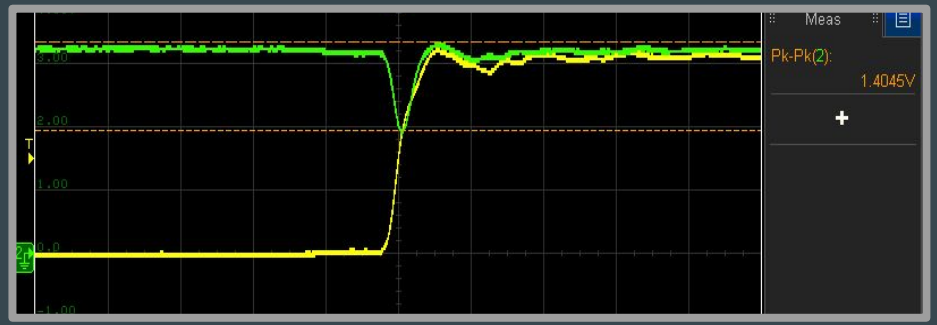


Rising Edge noise: ~864 mV

Voltage Collapse Quiet High:



Falling Edge noise: ~2.8 V



Rising Edge noise: ~1.4 V